In The Specification:

Please amend the specification with the following replacement paragraphs. No new matter is added by the amendments listed below:

Page 3, lines 18-20:

Figure 5A is a schematic top plan view of the copier control computer board including a control panel data cable connection.

Page 4, lines 10-12:

Figure 10A is a schematic top plan view of the copier control computer board including a copier control panel data cable connection with an active data tap.

Page 9, lines 24-31:

The single CPU based translator system for a static multiplexed data interface is displayed in FIGURE 7 and 8. It is microprocessor based using standard ~~off-the-self~~ off-the-shelf components as well as basic design techniques. A 6809 microprocessor chip is the central processing unit 22 (CPU) along with a programmable address decode 24 (16V8) used to select the support devices (i.e., RAM, ROM, etc.) that are address mapped to the CPU 22.

Page 11, lines 2-11:

The set of configuration selection switches 30 enables the translator 6 to take on different functional characteristics based on the setting of the switches 30. The ~~output~~ outputs of the switches 30 are read by the CPU 22 through a digital port. This device consists of three 8-bit parallel ports that are configured [[as]] to allow the CPU 22 to read in the digital level signals from the digital port 32. The ~~state~~ states of the switches 30 are read in at power-up time by the CPU 22 to set up certain operating characteristics of the translator 6.

Page 11, lines 30-35:

The output of the comparator 40, 0V for a logical "0" state of +5V for a logical "1" state, will reflect the differential relation of the voltage input from the copier 2 and VREF. That ~~is to say,~~ is, if the input is greater than the reference, the output will be 0V and ~~visa~~ vice versa.